In The Specification:

Please amend paragraphs [0023] and [0025] as follows:

[0023] Figure 4 shows the schematic drawing of the DDR termination array 16 of the present invention, which comprises a plurality of resistors, a plurality of signal terminals, a plurality of switches and an enable pin EN. Each of the resistors has a first terminal and a second terminal. The first terminals respectively connect with the voltage source V_{TT}, so that the resistors are functioned as termination resistors. The second terminals connect with relative signal terminals via switches. Each switch in the embodiment has a first terminal, a second terminal and a control terminal. All the first terminals connect with their corresponding signal terminals, respectively. The control terminals are coupled to the enable pin EN ~~that is used to determine whether all~~ which receives the control signal for controlling on/off of the switches ~~are conducted or not~~. When the enable pin delivers an enable state, the switches are conducted and the voltage source Vtt are coupled to the memory module in the memory module slot 14 ~~signals can be output from the signal terminals~~. When the enable pin EN delivers a disable state, the switches are open and the voltage source Vtt are not coupled to the memory module in the memory module slot 14 ~~to prevent signals from being output from associated signal terminals~~. The switches can be established by using transmission gates.

[0025] The invention also provides an operation method for the disclosed motherboard that further comprises a memory module slot and a termination resistor, wherein the termination resistor~~, the memory module slot~~ and the voltage source together form an operation circuitry. The operation method comprises the following steps. The operation circuitry will be cut off from

the memory module slot according to the indication of a control signal when the motherboard goes into the power saving mode or before the memory module is inserted into the memory module slot. When the motherboard returns to a normal operation mode and the memory module is inserted into the memory module slot, the operation circuitry will be connected to the memory module slot for operations according to the indication of the control signal. The cutting-off and connecting operations mentioned above is achieved by respectively cutting off and establishing associated connections between the termination resistors and the memory module slots or between the termination resistors and relative voltage source

In The Drawings:

Please substitute the attached clean drawing of Fig. 4 for the pending drawing of Fig. 4. The amended portion is the addition of the reference number "16".